UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/784,178	02/24/2004	Jang-Kun Song	6192.0164.C1	1140

7590 11/22/2004

McGuireWoods LLP
Suite 1800
1750 Tysons Boulevard
McLean, VA 22102

EXAMINER	
SCHECHTER, ANDREW M	
ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 11/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/784,178	SONG ET AL.	
	Examiner	Art Unit	
	Andrew Schechter	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *26,27,29-32 and 34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *26,27,29-32 and 34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/853,642.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Terminal Disclaimer

1. The terminal disclaimer filed on 2 November 2004 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of U.S. Application 09/853,642 has been reviewed and is NOT accepted.

2. The terminal disclaimer does not comply with 37 CFR 1.321(b) and/or (c) because:

> The application/patent being disclaimed has been improperly identified since the number used to identify the application being disclaimed is incorrect. The correct number is 09/853,642, which is now U.S. Patent No. 6,781,651.

Response to Arguments

3. Applicant's arguments filed 17 September 2004 have been fully considered but they are not persuasive.

As discussed above, the terminal disclaimer filed on 2 November 2004 does not overcome the previous double patenting rejections, which are repeated below.

The applicant argues [p. 7-8] that obvious-type double patenting rejections should only rely on the co-pending application, without the use of secondary references (*Han, Yanagisawa,* and *Murade*). This is not persuasive, as the secondary references serve to evidence the obviousness of the subject matter.

The applicant argues [p. 8-9] that *Yanagisawa* does not suggest the black matrix disconnected at portions between two adjoining gate lines, since there are no explicit

gate lines. This is not persuasive. *Yanagisawa* teaches having a black matrix disconnected at portions which, when combined with *Han*, would be between the two adjoining gate lines.

Claim Objections

4. Claim 29 is objected to because of the following informalities: "covering the disconnected portions of the black matrix" should be "covering the gap between the disconnected portions of the black matrix". Appropriate correction is required.

Double Patenting

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claim 26 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,781,651 (formerly claim 4 of copending Application No. 09/853,642) in view of *Yanagisawa,* U.S. Patent No. 5,128,786.

Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 26 is anticipated by claim 1, except for the amended limitation that the black matrix is disconnected at portions between the two adjoining gate lines. It would have been obvious to one of ordinary skill in the art at the time of the invention to have it so, since *Yanagisawa* teaches having the black matrix disconnected at portions between the two adjoining gate lines, since this reduces display defects which would otherwise be caused by short-circuits between the black matrix and the other electrodes [col. 2, lines 42-49].

7. Claims 27, 29, and 30 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,781,651 (formerly claim 4 of copending Application No. 09/853,642) in view of *Han et al.*, U.S. Patent No. 5,926,235, *Yanagisawa,* U.S. Patent No. 5,128,786, and *Murade,* U.S. Patent No. 6,297,862.

The additional limitations of claim 27 are disclosed by *Han*, and it would have been obvious to one of ordinary skill in the art at the time of the invention to do so, motivated by the necessity to electrically connect the pixel electrode to the drain electrode to thereby receive an electrical signal and the desire to place the pixel electrode on top of the passivation layer, in order to achieve greater aperture ratio and reduce stray capacitances among other reasons. The additional limitations of claim 29 are disclosed by claim 4, in the case of the buffer layer covering the (gap between) disconnected portions, and taught by *Yanagisawa* [see Fig. 7; it would have been obvious for the reasons given in the related discussion] in the case of the first and

second portions overlapped with the gate and data lines. The additional limitation of claim 30 would have been obvious to one of ordinary skill in the art at the time of the invention in view of *Murade*, as discussed in detail in the rejection under 35 U.S.C. 103 below.

8. Claim 31 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 3 of U.S. Patent No. 6,781,651 (formerly claim 18 of copending Application No. 09/853,642) in view of *Yanagisawa,* U.S. Patent No. 5,128,786.

Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 31 is anticipated by claim 3, except for the amended limitation that the black matrix is disconnected at portions between the two adjoining gate lines. It would have been obvious to one of ordinary skill in the art at the time of the invention to have it so, since *Yanagisawa* teaches having the black matrix disconnected at portions between the two adjoining gate lines, since this reduces display defects which would otherwise be caused by short-circuits between the black matrix and the other electrodes [col. 2, lines 42-49].

9. Claims 32 and 34 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 3 of U.S. Patent No. 6,781,651 (formerly claim 18 of copending Application No. 09/853,642) in view of *Han et al.*, U.S. Patent No. 5,926,235, *Yanagisawa,* U.S. Patent No. 5,128,786, and *Murade,* U.S. Patent No. 6,297,862.

Claims 32 and 34 are analogous to claims 27 and 30, and are similarly rejected.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Han et al.,* U.S. Patent No. 5,926,235 in view of *Yanagisawa,* U.S. Patent No. 5,128,786.

Han discloses [see Fig. 6, for instance] a liquid crystal display comprising a first insulating substrate [110], a gate line assembly [107] with gate lines and gate electrodes [see Fig. 4, 107 and 117], a gate insulating pattern [109], a semiconductor pattern [111], an ohmic contact layer [112], a data line assembly with source and drain electrodes [105 and 106] and data lines [115], and a protective layer [113a] covering the data line and gate line assemblies while exposing the gate insulating pattern, the semiconductor pattern, and the substrate below the gate insulating pattern (where the insulating layer is located in the claimed invention) at the pixel areas [compare Figs 6a and 6b with the application's Fig. 2].

Han does not disclose a black matrix formed on the substrate, mesh-shaped with opening portions at pixel areas and disconnected at portions between two adjoining gate lines, and an insulating layer on and covering the black matrix and substrate. *Yanagisawa* does disclose a black matrix [16] formed on an analogous substrate for an

analogous device, mesh-shaped with openings at the pixel areas and disconnected at portions between the horizontal parts of the black matrix (where the two adjoining gate lines in *Han* would be placed), and an insulating layer [17] on and covering the black matrix and substrate. The rest of the structure (electrodes, alignment layer, etc.) is then layered on top of this insulating layer. Note that although the figures in *Yanagisawa* depict a passive matrix LCD with simple lines of electrodes, *Yanagisawa* explicitly says that its invention (the black matrix in discontinuous portions, separated from the electrodes above by an insulating layer) "can also be applied to the liquid crystal display devices of the TFT active matrix type" [col. 8, lines 20-26]. It would therefore have been obvious to one of ordinary skill in the art at the time of the invention to form the black matrix and insulating layer of *Yanagisawa* under the gate electrode structure of *Han*, motivated by *Yanagisawa's* teachings that the use of a black matrix prevents light from "leaking through the net-like area ... between the image elements" [col. 1, lines 14-23] so a black matrix is beneficial, and that the use of this particular black matrix (discontinuous, with various portions) reduces display defects which would otherwise be caused by short-circuits between the black matrix and the other electrodes [col. 2, lines 42-49]. Claim 26 is therefore unpatentable.

Han also discloses a pixel electrode [104] connected to the drain electrode, the contact made through a first contact hole [116] in the protective layer. Claim 27 is therefore also unpatentable.

12. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Han et al.*, U.S Patent No. 5,926,235 in view of *Yanagisawa*, U.S. Patent No. 5,128,786 as

applied to claims 26 and 27 above, and further in view of *Murade,* U.S. Patent No. 6,297,862.

The additional limitation is that the pixel electrode has a peripheral portion overlapping the black matrix. *Han* does not disclose a black matrix. *Yanagisawa* discloses a black matrix [see Figs. 6-9] which overlaps its transparent display electrodes (where the pixel electrode would be in an active matrix device), but does not explicitly disclose a pixel electrode or give a teaching explaining why it is beneficial to have the black matrix and the transparent display electrodes overlap as they are depicted doing.

Murade discloses an active matrix LCD with a pixel electrode [14] and a black matrix [7] on the substrate, separated from the other electrodes by an insulating layer [11], analogous to both *Yanagisawa* and the present invention. (The black matrix in *Murade* is also divided into portions.) *Murade* discloses that the black matrix overlaps the pixel electrode [col. 14, lines 66-67] and teaches that this arrangement dispenses with the need for precise alignment of a black matrix on the opposite substrate, and that the thus obtained liquid crystal devices show little variation in light transmittance [col. 14, line 47 – col. 15, line 17]. It would therefore have been obvious to one of ordinary skill in the art at the time of the invention to overlap the pixel electrode and the black matrix, motivated by the example and teaching of *Murade*. Claim 30 is therefore unpatentable.

13. Claims 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Han et al.,* U.S. Patent No. 5,926,235 in view of *Yanagisawa,* U.S. Patent No. 5,128,786, and further in view of *Ishiguro*, U.S. Patent No. 5,956,103.

Han discloses [see Fig. 6, for instance] a method for fabricating a TFT substrate for a liquid crystal display comprising having a first insulating substrate [110], forming a gate line assembly [107] with gate lines and gate electrodes [see Fig. 4, 107 and 117], depositing a gate insulating pattern [109], a semiconductor pattern [111], forming an ohmic contact layer [112], a data line assembly with source and drain electrodes [105 and 106] and data lines [115], depositing a protective layer [113a] covering the data line and gate line assemblies, and forming opening portions exposing the substrate (where the insulating layer is located in the claimed invention) through patterning the protective layer, the gate insulating pattern, and the semiconductor pattern [compare Figs 6a and 6b with the application's Fig. 2].

Han does not disclose a black matrix formed on the substrate, mesh-shaped with opening portions at pixel areas and disconnected at portions between two adjoining gate lines, and an insulating layer on and covering the black matrix and substrate. *Yanagisawa* does disclose a black matrix [16] formed on an analogous substrate for an analogous device, mesh-shaped with openings at the pixel areas and disconnected at portions between the horizontal parts of the black matrix (where the two adjoining gate lines in *Han* would be placed), and an insulating layer [17] on and covering the black matrix and substrate. The rest of the structure (electrodes, alignment layer, etc.) is then layered on top of the insulating layer. Note that although the figures in *Yanagisawa* depict a passive matrix LCD with simple lines of electrodes, *Yanagisawa* explicitly says that its invention (the black matrix in discontinuous portions, separated from the electrodes above by an insulating layer) "can also be applied to the liquid crystal display

devices of the TFT active matrix type" [col. 8, lines 20-26]. It would therefore have been obvious to one of ordinary skill in the art at the time of the invention to form the black matrix and insulating layer of *Yanagisawa* under the gate electrode structure of *Han*, motivated by *Yanagisawa's* teachings that the use of a black matrix prevents light from "leaking through the net-like area ... between the image elements" [col. 1, lines 14-23] so a black matrix is beneficial, and that the use of this particular black matrix (discontinuous, with various portions) reduces display defects which would otherwise be caused by short-circuits between the black matrix and the other electrodes [col. 2, lines 42-49].

Han also does not disclose that the gate lines and data lines are narrower than the black matrix. This is not taught by either *Han* or *Yanagisawa*, since it compares two features, one from each reference. However, *Ishiguro* teaches that "a black matrix is provided to prevent light from leaking from the periphery of each pixel electrode ... [and] is typically formed with margins to ensure that no light leaks from the periphery of each pixel electrode" [col. 1, lines 31-35]. (Also note again *Yanagisawa's* teaching above regarding the use of a black matrix to prevent light leaking through "between image elements", in this case the pixel electrodes.) Thus, a purpose of the black matrix is to cover the gaps between the display electrodes in a passive matrix display (as shown in *Yanagisawa*), or the gaps between the pixel electrodes in an active matrix display (as in *Han*), to prevent light leakage and improve the display quality. As can be seen in *Han,* the width of the gate and data lines is less than the gaps between the pixel electrodes which are to be covered by the black matrix. It would therefore have been obvious to

one of ordinary skill in the art at the time of the invention to have the black matrix wider than the gate lines and the date lines, motivated by the desire to have the black matrix cover the pixel electrode periphery and ensure that no light leaks through, as taught by *Ishiguro*. Claim 31 is therefore unpatentable.

Han also discloses forming a pixel electrode [104] connected to the drain electrode, the contact made through a first contact hole [116] in the protective layer. Claim 32 is therefore also unpatentable.

14. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Han et al.,* U.S. Patent No. 5,926,235,*Yanagisawa,* U.S. Patent No. 5,128,786, and *Ishiguro*, U.S. Patent No. 5,956,103 as applied to claims 31 and 32 above, and further in view of *Murade,* U.S. Patent No. 6,297,862.

The additional limitation is that the pixel electrode has a peripheral portion overlapping the black matrix. *Han* does not disclose a black matrix. *Yanagisawa* discloses a black matrix [see Figs. 6-9] which overlaps its transparent display electrodes (where the pixel electrode would be in an active matrix device), but does not explicitly disclose a pixel electrode or give a teaching explaining why it is beneficial to have the black matrix and the transparent display electrodes overlap as they are depicted doing.

Murade discloses an active matrix LCD with a pixel electrode [14] and a black matrix [7] on the substrate, separated from the other electrodes by an insulating layer [11], analogous to both *Yanagisawa* and the present invention. (The black matrix in *Murade* is also divided into portions.) *Murade* discloses that the black matrix overlaps the pixel electrode [col. 14, lines 66-67] and teaches that this arrangement dispenses

with the need for precise alignment of a black matrix on the opposite substrate, and the thus obtained liquid crystal devices show little variation in light transmittance [col. 14, line 47 – col. 15, line 17]. It would therefore have been obvious to one of ordinary skill in the art at the time of the invention to overlap the pixel electrode and the black matrix, motivated by the example and teaching of *Murade*. Claim 34 is therefore unpatentable.

Allowable Subject Matter

15. Claim 29 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, if the double patenting rejection were also overcome.

16. The following is a statement of reasons for the indication of allowable subject matter:

The prior art, excepting U.S. Patent No. 6,781,651 (see the double patenting rejection above), does not disclose the additional limitation of a buffer layer covering the (gaps between) the disconnected portions of the black matrix. Claim 29 would therefore be allowable if rewritten appropriately, if the double patenting rejection were overcome.

Conclusion

17. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Schechter whose telephone number is (571) 272-2302. The examiner can normally be reached on Monday - Friday, 9:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on (571) 272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Andrew Schechter
Patent Examiner
Technology Center 2800
15 November 2004